REMARKS

Former Claims 1-8 are kept unchanged except for minor typography errors in claim 8 (wherein the word "input" has been substituted by the word "output"). Thus, Claims 1-8 as amended in the office action dated April 23, 2003 are pending in the present application.

Claim rejection under 35 USC §112:

Claims 1-8 have been rejected under 35 U.S.C. 112 first paragraph, as failing to comply with the written description requirement.

The Examiner states that nothing in the Specification discloses that as a first step a die is to be secured to a substrate while said substrate already comprises at least one input matching element and at least one input signal lead.

Applicants respectfully disagree with the Examiner on that point. The present invention aims at providing a simple and accurate efficient way of manufacturing a power transistor circuit. The efficiency of the present invention rests on the fact that the inductance parameter for each wire can be determined during the test by a test network. This efficient way consists in using a test network to measure **a performance characteristic of the transistor before connecting the transistor with the input matching element and input signal lead** as is mentioned on page 10, lines 5-12. This test network has connections with known inductances to electrically couple the transistor input terminal to an input matching element, an input signal lead, or both; and set the impedance of one or more connections based at least in part on the measured transistor performance characteristic.

The transistor having an input terminal is embedded in a die that is secured to a substrate comprising at least one input matching element and at least one input signal lead. It does not matter whether the die is secured to the substrate before the at least one input matching element and the at least one input signal lead or vice versa. What is important is that these elements, meaning the transistor, at least one input matching element and at least one input signal lead, have to be secured on the die before measuring the performance characteristic of the

transistor. Therefore, the chronological order in which the transistor, the input signal lead or the input matching element are secured to the susbstrate does not matter. A person skilled in the art would readily understand this fact from the present specification. Claims 1 and 5 contain subject matter which are described in the specification in such a way as to reasonably convey to one skilled in the relevant art how to carry out the invention.

That is the reason why step (1) of claim 1 which states "securing a die to a substrate, the die comprising a transistor having an input terminal, the substrate comprising at least one input matching element and at least one input signal lead", does not specify the chronological order of how these elements are secured as long as they are secured before the measurement of the performance characteristic of step (2).

Similarly, the test network also measures a performance characteristic of the transistor output before connecting the transistor with the output matching element and output signal lead, which is covered by claim 5.

Therefore, in order to measure a performance characteristic of the transistor, the die is placed on a substrate carrying at least one input matching element and input signal lead. At this time no connections are established between these elements. It is only at the next step (2) of claim 1 or claim 5, that a test network is used to simulate the connections and measure characteristics of the power transistor circuit. The test network comprises connectors with known inductances to establish the respective connections during the measurement. Fig. 6 of the present specification shows an example how a test network is placed on a unwired transistor circuit for testing purposes. Once the measurement has been conducted, the respective necessary inductances for each connection is determined and wiring of the different elements is performed with wires having the respectively determined inductances. Therefore, the claims contain subject matter which are described in the specification in such a way as to reasonably convey to one skilled in the relevant art how to carry out the invention.

CONCLUSION

As hereby amended, claims 1-8 are pending in the application and they are patentable under 35 U.S.C. 112 first paragraph. Therefore, applicants respectfully request withdrawal of the rejection and allowance of all pending claims.

Applicants do not believe that any other fees are due at this time; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to this document, the Commissioner is authorized to deduct the fees from Deposit Account No. 02-0383, *(formerly Baker & Botts, L.L.P.)* Order Number 071308.0168.

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Claim Amendment Version With Markings to Show Changes

1. (previously amended) A method of manufacturing a power transistor circuit, comprising carrying out the following steps in the enumerated order:

(1) securing a die to a substrate, the die comprising a transistor having an input terminal, the substrate comprising at least one input matching element and at least one input signal lead;

(2) measuring a performance characteristic of the transistor before connecting the transistor with the input matching element and input signal lead by means of a test network comprising connections with known inductances;

(3) using one or more wires to electrically couple the transistor input terminal to an input matching element, an input signal lead, or both; and

(4) setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic from step (2).

2. (previously amended) The method of claim 1, wherein the performance characteristic is defined, at least in part, by one or more of input capacitance, impedance, gain flatness, and signal phase shift.

3. (previously amended) The method of claim 1, wherein the impedance of the one or more wires is set by selecting a number of wires used to make at least one electrical connection of the transistor circuit.

4. (previously amended) The method of claim 1, wherein the impedance of the one or more wires is set by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.

5. (currently amended) A method of manufacturing a power transistor circuit, comprising carrying out the following steps in the enumerated order:

(1) securing a die to a substrate, the die comprising a transistor having an output terminal, the substrate comprising at least one [input] **output** matching element and at least one [input] **output** signal lead;

(2) measuring a performance characteristic of the transistor before connecting the transistor with the [input] **output** matching element and [input] **output** signal lead by means of a test network comprising connections with known inductances;

(3) using one or more wires to electrically couple the transistor output terminal to an output matching element, an output signal lead, or both; and

(4) setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic from step (2).

6. (previously amended) The method of claim 5, wherein the performance characteristic is defined, at least in part, by one or more of output capacitance impedance, gain flatness, and signal phase shift.

7. (previously amended) The method of claim 5, wherein the impedance of the one or more wires is set by selecting a number of wires used to make at least one electrical connection of the transistor circuit.

8. (previously amended) The method of claim 5, wherein the impedance of the one or more wires is set by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.